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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,350	PORTER ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21* is/are allowed.

6)☒ Claim(s) *1-14 and 16-20* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendments filed on 15 November 2004.

Claim Objections

2. Claims 9, and 20 are objected to because of the following informalities:

3. In the claim 9, line 3, the abbreviation " ISI " needs to be defined at least once in claim.

4. In the claim 20, line 1, the abbreviation " SCSI " needs to be defined at least once in claim.

Appropriate correction is required.

5. In response to applicant's request for clarification the signals A, NA, and B, NB in Kuo [US Patent 6,377,095] are complementary signals [col. 7, lines 33 – 34].

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 – 10, and 17 – 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chaudhry et al. [hereinafter as Chaudhry], US Patent 6,310,569 B1.

8. As to claim 1, Chaudhry an apparatus comprising:

a. a first plurality of parallel switches [transistors as shown in fig. 2] configured to (i) each receive a multiphased ['high' and 'Low'] data signal [D digital input data signal] and (ii) control a voltage on a first output pin [Q]; and

b. a second plurality of parallel switches [transistors as shown in fig. 2] configured to (i) each receive a digital complement [DB complementary signal of D] of said multiphased ['high' and 'Low'] data signal [D digital input data signal] and (ii) control a voltage on a second output pin [QB], wherein said first and second pluralities of parallel switches are configured to provide rise time control [to provide same rise and fall time] of a differential waveform [col. 2, lines 35 – 67, fig.2].

9. As to claim 19, Chaudhry an apparatus comprising:

a. means [transistors] for controlling a voltage on a first output pin [Q] with a first plurality of parallel switches [transistors as shown in fig. 2] each receiving a multiphased ['high' and 'Low'] data signal [D digital input data signal];

b. means [transistors] for controlling a voltage on a second output pin [QB] with a second plurality of parallel switches [transistors as shown in fig. 2] each receiving a digital complement of said multiphased ['high' and 'Low'] data signal [DB complementary signal of D]; and

c. means [40, 41 pull up transistors] for providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal [col. 2, lines 35 – 67, col. 3, lines 1 – 67, col. 4, lines 1 – 16, fig.2].

10. As to claim 20 Chaudhry discloses a method for implementing SCSI equalization [skewless] comprising steps of:

a. controlling a voltage on a first output pin [Q] with a first plurality of parallel switches [transistors as shown in fig. 2] each receiving a multiphased ['high' and 'Low'] data signal [D digital input data signal];

b. controlling a voltage on second output pin [QB] with a second plurality of parallel switches [transistors as shown in fig. 2] each receiving a digital complement [DB] of said multiphased ['high' and 'Low'] data signal [DB complementary signal of D]; and

c. providing rise time control a differential waveform, wherein said first and second pluralities of parallel switches [transistors] are driven by a phased data signal [col. 2, lines 35 – 67, col. 3, lines 1 – 67, col. 4, lines 1 – 16, fig.2].

11. As to claim 2, Chaudhry discloses a first [rising] and last phase [falling] of multiphased data signal [D, DB] is configured to determine a rise and fall time [differential switching scheme minimizes time skew and gives same rise and fall time] of said differential wave form [differential signal] [col. 2, lines 35 – 50, fig. 2].

10. As to claim 3, Chaudhry discloses a first [48] and second [49] pluralities of parallel switches [transistors, fig. 2] are weighed [by controlling voltage/current and turning on/off transistors] to determine a pulse shape of differential wave form [differential signal][Q, QB] [col. 3, lines 1 –67, fig. 2].

12. As to claims 4, 5, and 6, Chaudhry discloses one or more sources [70, 84, fig. 4 - 5] parallel and configured to provide current to each of first [PMOS] and second [NMOS] pluralities of parallel switches [transistors] and current sources [70, 84] are weighed [by controlling voltage/current and turning on/off transistors] to determine a pulse shape of differential wave form [Q, QB] [col. 1, lines 5 - 14, tig. 31 [col. 3, lines 1 –67, fig. 2 - 5].

13. As to claim 7, Chaudhry discloses a first driver [33] configured in parallel; and a second driver [32] configured in parallel [as shown in fig. 3], wherein said first [33] and second [32]

drivers are configured to synchronize to a phased clock signal [CK, clock signal][col. 3, lines 1 – 3, col. 3, lines 45 – 47, fig. 3].

14. As to claim 8, Chaudhry discloses a first [33] and second [32] drivers are configured to perform pre-emphasis on said differential waveform [D, DB differential input signal] [col. 3, lines 1 – 13, col. 3, lines 45 – 47, fig. 3].

15. As to claim 9, Chaudhry discloses a first [33] and second [32] drivers are configured to mitigate effects of ISI [col. 3, lines 1 – 13, col. 3, lines 45 – 47,][fig. 3].

16. As to claim 10, Chaudhry discloses the apparatus with first driver [33] comprises a main driver [which passes ONE] and said second driver [32] comprises a secondary driver [which passes ZERO][col. 3, lines 1 – 13, col. 3, lines 45 – 47, fig. 3].

17. As to claim 17, Chaudhry discloses a differential switch driver apparatus according to claim wherein said apparatus configured to overcome cable induced effects [minimizes skew][col. 3, lines 45 – 47].

18. As to claim 18, Chaudhry discloses drivers [33, 32] with clock signal [CK] configured to synchronize a plurality of drivers [42, 35, 44, 37] to provide precompensation [fig.3].

19. Claims 1 – 14, and 17 – 20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kuo, US Patent 6,377,095 [cited in previous office action].

20. As to claim 1, Kuo discloses an apparatus [differential line driver, fig. 1] and method [for controlling rise and fall time] [for controlling rise and fall time] comprising:

a. a first plurality of parallel switches [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] configured to (i) each receive a multiphased data signal [data signal

with 'high' and 'low'] and (ii) control a voltage [by turning on and off transistors with controlled current and delay time] on a first output pin [D+]; and

b. a second plurality of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] configured (i) each receive a digital complement of said multiphased data signal [A, NA, and B, NB are complementary pair] and (ii) to control a voltage [by turning on and off transistor with controlled current and delay time] on a second output pin [D-], wherein said first [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] and second [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] pluralities of parallel switches are configured to provide rise time control [controlling rise and fall time] of a differential waveform [D+, D-] and are driven by [N parallel drivers] phased data signal [DATA_IN] [col. 1, lines 6 – 8, lines 53 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 51, col. 4, lines 12 – 61, col. 7, lines 32 – 34, fig.1, 3, and 5 – 6].

21. As to claim 19, Kuo discloses an apparatus [differential line driver, fig. 2] and method [for controlling rise and fall time] [for controlling rise and fall time] comprising:

a. means [driver circuit] for controlling a voltage [by turning on and off transistors with controlled current and delay time] on a first output pin [D+] with a first plurality of parallel switches [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] each receiving a multiphased data signal [data signal with 'high' and 'low'];

b. means [driver circuit] controlling a voltage [by turning on and off transistors with controlled current and delay time] on a second output pin [D-] with a second plurality of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] each receiving

a digital complement [A, NA, and B, NB are complementary pair] of said multiphased data signal [data signal with 'high' and 'low']; and

c. means [bias circuit] for providing rise time control [controlling rise and fall time] of a differential waveform [D+, D-], wherein first [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] and second pluralities of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] are driven by [N parallel drivers] a phased data signal [DATA_IN] [col. 1, lines 6 – 8, lines 53 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 51, col. 4, lines 12 – 61, fig. 1, 3, and 5 – 6].

22. As to claim 20, Kuo discloses an apparatus [differential line driver, fig. 1] and method [for controlling rise and fall time] comprising:

(A) controlling a voltage [by turning on and off transistors with controlled current and delay time] on a first output pin [D+] with a first plurality of parallel switches [switches as shown 210, 224 in fig.2, and 230 in fig. 5] each receiving a multiphased data signal [data signal with 'high' and 'low'];

(B) controlling a voltage [by turning on and off transistors with controlled current and delay time] on second output pin [D-] with a second plurality of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] each receiving a digital complement [A, NA, and B, NB are complementary pair] of said multiphased data signal [data signal with 'high' and 'low']; and

(C) providing rise time control [controlling rise and fall time] of a differential waveform [D+, D-], wherein said first [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] and second pluralities of parallel switches [N parallel driver cells as in fig. 3, each

having MNA, MNB, as in fig.5] are driven by [N parallel drivers] a phased data signal [DATA_IN] [col. 1, lines 6 – 8, lines 53 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 51, col. 4, lines 12 – 61, fig. 1, 3, and 5 – 6].

23. As to claim 2, Kuo discloses a first [rising] and last phase [falling] of phased data signal [DATA_IN] is configured to determine a rise and fall time [by determining current level bias] of differential wave form [D+, D-][col. 2, lines 56 – 67, col. 3, lines 1 – 36].

24. As to claim 3, Kuo discloses a first [MA, MB] and second [MNA, MNB] pluralities of parallel switches [in N parallel drivers] are weighed [by controlled current] to determine a pulse shape [by determining the current level bias] of differential wave form [D+, D-] [col. 1, lines 5 – 14, fig. 3].

25. As to claims 4, 5, and 6, Kuo discloses one or more sources [IS1, IS2, fig. 9] parallel and configured to provide current to each of first and second pluralities of parallel switches and current sources are weighed [by controlled current] to determine a pulse shape [by determining the current level bias] of differential wave form [D+, D-] [col. 1, lines 5 – 14, fig. 3] [col. 3, lines 17 – 41, fig. 3, 6, 9].

26. As to claim 7, Kuo discloses a first driver configured in parallel; and second driver configured in parallel, wherein said first and second drivers are configured to synchronize to a phased clock signal [CLOCK][col. 5, lines 33 – 53] [fig. 1 - 3].

27. As to claim 8, Kuo discloses first [data shaper] and second [edge rate control logic] drivers configured to perform pre-emphasis [reshapes based upon clock] on differential waveform [col. 1, lines 5 – 14, fig. 1, 3].

28. As to claim 9, as Kuo discloses an apparatus [differential line driver] to drive differential signal with drivers [N parallel drivers] and driver bias circuit [BIAS circuit] to control the current with mirrored current technique to generate differential output which inherently teaches to mitigate the ISI effects [glitches][col. 3, lines 46 – 52].

29. As to claim 10, Kuo discloses first driver [data shaper] comprises a main driver and second driver [edge rate control logic] comprises a secondary driver [N parallel driver] [fig. 3].

30. As to claim 11, Kuo discloses first driver [data shaper] and second driver [edge rate control logic] comprises one or more flip-flops [latches][fig. 3].

31. As to claim 12, Kuo discloses first and second drivers clocked by [CLOCK] a multiphase [inherent property of clock signal] clock signal [fig. 3].

32. As to claims 13, and 14, Kuo discloses a clock [data clock] generation signal [D+, D-] configured to generate multiphase clock [D+, D-] in response to a data signal [D1, D2] and a precompensation signal [PBIAS1, PBIAS2][fig. 1 - 3].

33. As to claim 17, Kuo discloses that an apparatus [differential line driver] is configured to overcome cable induced [glitch] effects [col.3, lines 48 – 52].

34. As to claim 18, Kuo discloses an apparatus [differential line driver] configured to synchronize [by producing a first and second control signals skewed in time by a time delay] a plurality of drivers to provide precompensation [col. 4, lines 19 – 30].

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claim 11 – 14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaudhry et al. [hereinafter as Chaudhry], US Patent 6,310,569 B1 as applied to claims 1 – 10 above, and further in view of Kenney et al. [hereinafter as Kenney], US Patent 5,008,563.

37. As to claim 11, Chaudhry an apparatus comprising: a first plurality of parallel switches [transistors as shown in fig. 2] configured to control a voltage on a first output pin; a second plurality of parallel switches [transistors as shown in fig. 2] configured to control a voltage on a second output pin, wherein said first and second pluralities of parallel switches are configured to provide rise time control of a differential waveform [col. 2, lines 46 – 51] and are driven by a phased data signal [D, DB]; a first driver and a second driver [differential switch driver] configured in parallel [fig. 2], wherein said first and second drivers (i) are configured to synchronize to a phased clock signal [CK, clock]] and (ii) are clocked by multiphased clock signal [CK clock signal] [col. 2, lines 35 – 67, col. 3, lines 1 – 67, col. 4, lines 1 – 16, fig.2].

However, Chaudhry discloses a first driver [33] and second driver [32] and a use of clock signal [CK] but he does not disclose that the first driver comprises one or more flip-flops and second driver comprises one or more flip-flops, and a clock generation circuit to generate multiphased clock in response to data signal and a precompensation signal. In summary, Chaudhry does not disclose the first and second driver comprising of one or more flip-flops and a clock generation circuit.

Kenney teaches an adjustable clock generator circuit to adjust the skew of the signals driving the clamp and sample switches with complementary clock generators [12, 16] with inputs [PH1, PH2] and width and position adjust signals [fig. 3]. Each of clock generators [12, 14, 16,

and 18] is identical in construction comprised of a D flip-flop [20, fig. 4], two adjustable rise time inverters [22, 24], two Schmitt triggers [26, 28] [col. 222 – 58, col. 2, lines 60 0 67, col. 3, lines 1 – 58 fig. 2 - 4].

It would have been obvious to one of ordinary skill in art, having the teachings of Chaudhry and Kenney before him at the time of invention was made, to modify the differential switching scheme disclosed by Chaudhry to include an adjustable clock generation circuit as taught by Kenney in order to obtain an apparatus with improved adjustable clock generator circuit causing signals to appear on complementary outputs having a pulse position controlled by the level of the first bias voltage and a width controlled by the level of second bias voltage with adjustable rise time inverter [col. 1, lines 25 – 58].

38. As to claim 12, Kenney discloses an apparatus with first [12] and second drivers [16] are clocked by a multiphase clock signal [PH1, PH2][fig. 3].

39. As to claim 13, Kenney discloses a clock generation circuit [fig. 4] configured to generate multiphase clock [Q, /Q] in response to a data signal [input clock] and a precompensation signal [VBIAS][fig. 4][col. 3, lines 16 – 39].

40. As to claim 14, Kenney discloses a clock generation circuit [fig. 4] is configured to generate said multiphase clock [q, /Q] in response to a data transaction on said data signal [input clock changes][col. 3, lines 16 – 39].

Response to Arguments

41. Applicant's arguments filed on 15 November have been fully considered but they are not persuasive.

42. Applicant has asked for clarification of the examiner's reading of Kuo for the input of the plurality of switches. In response to that, **singals A, NA, B, NB which are complementary signals as claimed,** col. 7, lines 31 - 33.

43. In reference to applicant's arguments on page 9 in particular, the Examiner points to FIGS. 3 and 5, of Kuo as relating to both the claimed first plurality of switches and the claimed second plurality of claimed switches. Applicant has argued that upon a closer examination, the devices MA, and MB of Kuo cannot be the claimed first plurality switches since they receive different signals. Examiner disagrees as **MA, MNA, MB, and MNB in fig. 5 are receiving singals A, NA, B, NB which are complementary signals as claimed,** col. 7, lines 31 - 33. Applicant further argues that the switch MA receives a signal A and the switch MB receives a signal In contrast, the claimed first plurality of switches are configured to each receive the multiphase data signal. Similarly, the switch MNA of Kuo receives the signal NA and the switch MNB receives the signal NB. In contrast, the claimed second plurality of switches are each configured to receive a digital complement of the multiphased data signal. Examiner disagrees as **singals A, NA, B, NB which are complementary signals as claimed,** col. 7, lines 31 - 33.

44. Applicant's arguments with respect to claims 1 - 20 for Groen have been considered but are moot in view of the new ground(s) of rejection.

45. Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references

in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

46. Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Allowable Subject Matter

47. Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

48. Claim 21 is allowed.

Conclusion

49. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
December 6, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100